

FDMC8200

Dual N-Channel PowerTrench[®] MOSFET 30 V, 9.5 m Ω and 20 m Ω

Features

- Q1: N-Channel
- Max $r_{DS(on)} = 20 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 6 \text{ A}$
- Max $r_{DS(on)}$ = 32 m Ω at V_{GS} = 4.5 V, I_D = 5 A

Q2: N-Channel

- Max $r_{DS(on)}$ = 9.5 m Ω at V_{GS} = 10 V, I_D = 9 A
- Max $r_{DS(on)}$ = 13.5 m Ω at V_{GS} = 4.5 V, I_D = 7 A
- RoHS Compliant

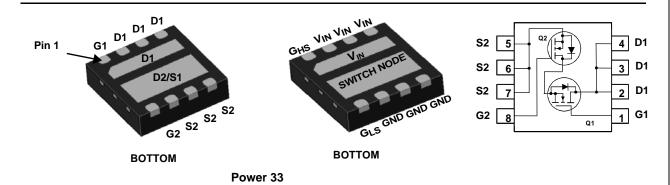


General Description

This device includes two specialized N-Channel MOSFETs in a dual Power33 (3mm x 3mm MLP) package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous MOSFET (Q2) have been designed to provide optimal power efficiency.

Applications

- Mobile Computing
- Mobile Internet Devices
- General Purpose Point of Load



MOSFET Maximum Ratings T_C = 25 °C unless otherwise noted

Symbol	Parameter			Q2	Units
V _{DS}	Drain to Source Voltage		30	30	V
V _{GS}	Gate to Source Voltage	(Note 3)	±20	±20	V
ID	Drain Current - Continuous (Package limited)	T _C = 25 °C	18	18	
	- Continuous (Silicon limited)	T _C = 25 °C	23	45	_
	- Continuous	T _A = 25 °C	8 ^{1a}	12 ^{1b}	- A
	- Pulsed		40	40	_
P _D	Power Dissipation	T _A = 25 °C	1.9 ^{1a}	2.2 ^{1b}	W
	Power Dissipation	T _A = 25 °C	0.7 ^{1c}	0.9 ^{1d}	vv
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to	+150	°C

Thermal Characteristics

R_{\thetaJA}	Thermal Resistance, Junction to Ambient	65 ^{1a}	55 ^{1b}	
$R_{ ext{ heta}JA}$	Thermal Resistance, Junction to Ambient	180 ^{1c}	145 ^{1d}	°C/W
$R_{ ext{ heta}JC}$	Thermal Resistance, Junction to Case	7.5	4	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8200	FDMC8200	Power 33	13 "	12 mm	3000 units

June 2009

FDMC8200
Dual
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Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units
Off Chara	cteristics						
BV _{DSS}	Drain to Source Breakdown Voltage	$ I_D = 250 \ \mu A, \ V_{GS} = 0 \ V \\ I_D = 250 \ \mu A, \ V_{GS} = 0 \ V $	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \ \mu$ A, referenced to 25 °C $I_D = 250 \ \mu$ A, referenced to 25 °C	Q1 Q2		14 14		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current		Q1 Q2			1 1	μA
I _{GSS}	Gate to Source Leakage Current	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$	Q1 Q2			100 100	nA nA
On Chara	cteristics						
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \ \mu A$ $V_{GS} = V_{DS}, I_D = 250 \ \mu A$	Q1 Q2	1.0 1.0	2.3 2.3	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \ \mu$ A, referenced to 25 °C $I_D = 250 \ \mu$ A, referenced to 25 °C	Q1 Q2		-5 -6		mV/°C
r _{DS(on)}	Static Drain to Source On Resistance		Q1		16 24 22	20 32 28	- mΩ
			Q2		7.3 9.5 10	9.5 13.5 13	
9 _{FS}	Forward Transconductance	$V_{DD} = 5 \text{ V}, \ I_D = 6 \text{ A}$ $V_{DD} = 5 \text{ V}, \ I_D = 9 \text{ A}$	Q1 Q2		29 56		S
Dynamic	Characteristics						
C _{iss}	Input Capacitance		Q1 Q2		495 1180	660 1570	pF
C _{oss}	Output Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		145 330	195 440	pF
C _{rss}	Reverse Transfer Capacitance		Q1 Q2		20 30	30 45	pF
R _g	Gate Resistance		Q1 Q2		1.4 1.4		Ω
Switching	g Characteristics						
t _{d(on)}	Turn-On Delay Time	Q1	Q1 Q2		11 13	20 23	ns
t _r	Rise Time	$V_{DD} = 15 \text{ V}, \text{ I}_{D} = 1 \text{ A},$ $V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$	Q1 Q2		3.1 4	10 10	ns
t _{d(off)}	Turn-Off Delay Time	Q2 V _{DD} = 15 V, I _D = 1 A,	Q1 Q2		35 38	56 60	ns
t _f	Fall Time	$V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$	Q1 Q2		1.3 6	10 12	ns
			-				

Total Gate Charge

Total Gate Charge

Gate to Source Charge

Gate to Drain "Miller" Charge

Q_{g(TOT)}

Q_{g(TOT)}

 Q_gs

 Q_{gd}

2

 $V_{GS} = 0 V$ to 10 V

 $V_{GS} = 0 V$ to 4.5 V

Q1:

Q2:

V_{DD} = 15 V,

V_{DD} = 15 V, I_D = 9 A,

I_D = 6 A,

Q1

Q2

Q1

Q2

Q1

Q2

Q1

Q2

7.3

16

3.1

7

1.8

4.1

1

1.5

10

22

4.3

10

nC

nC

nC

nC

FDMC8200
) Dual N
N-Channel F
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h [®] MOSFET

Symbol	Parameter	Test Conditions		Туре	Min	Тур	Max	Units
Drain-So	urce Diode Characteristics							
V _{SD}	Source to Drain Diode Forward Volt- age	00 / 0	(Note 2) (Note 2)	Q1 Q2		0.8 0.8	1.2 1.2	V
t _{rr}	Reverse Recovery Time	Q1 I _F = 6 A, di/dt = 100 A/µs		Q1 Q2		13 21	24 34	ns
Q _{rr}	Reverse Recovery Charge	Q2 I _F = 9 A, di/dt = 100 A/µs		Q1 Q2		2.3 5.6	10 12	nC

Notes:

1. R_{0JA} is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0JC} is guaranteed by design while R_{0CA} is determined by the user's board design.

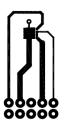


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c. 180 °C/W when mounted on a minimum pad of 2 oz copper

a.65 °C/W when mounted on a 1 in $^2\,$ pad of 2 oz copper



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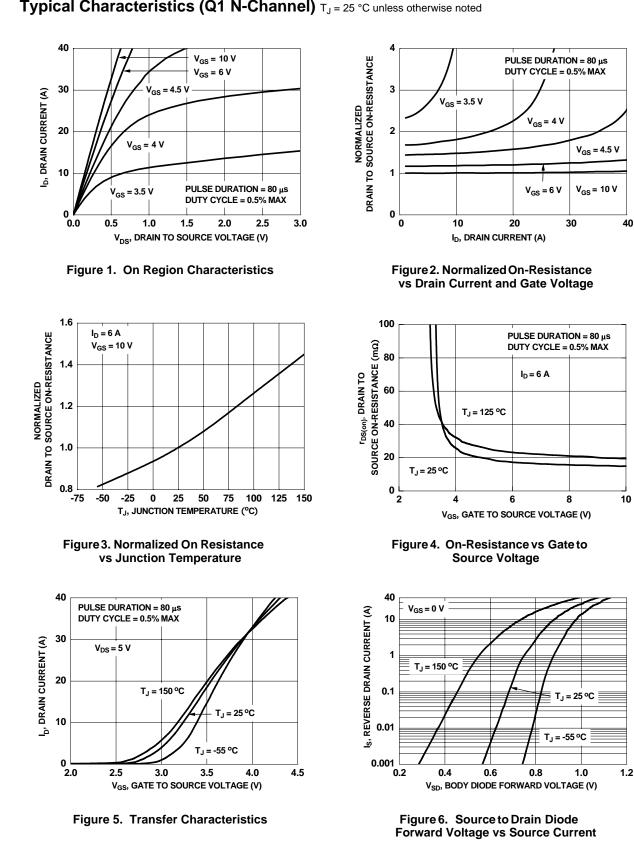
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d. 145 °C/W when mounted on a minimum pad of 2 oz copper

b.55 °C/W when mounted on a 1 in² pad of 2 oz copper

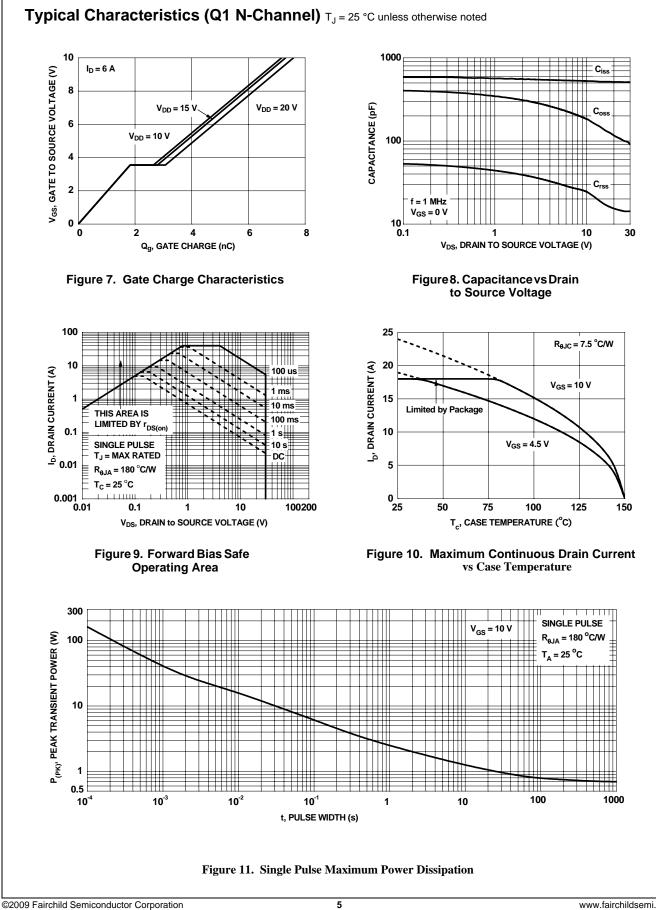
2. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.

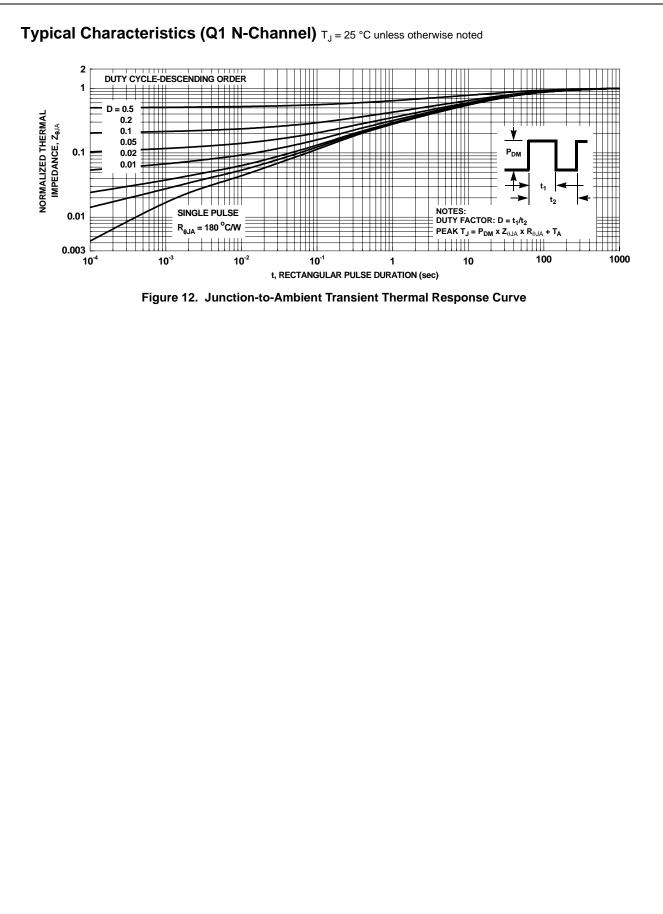
3. As an N-ch device, the negative Vgs rating is for low duty cycle pulse ocurrence only. No continuous rating is implied.



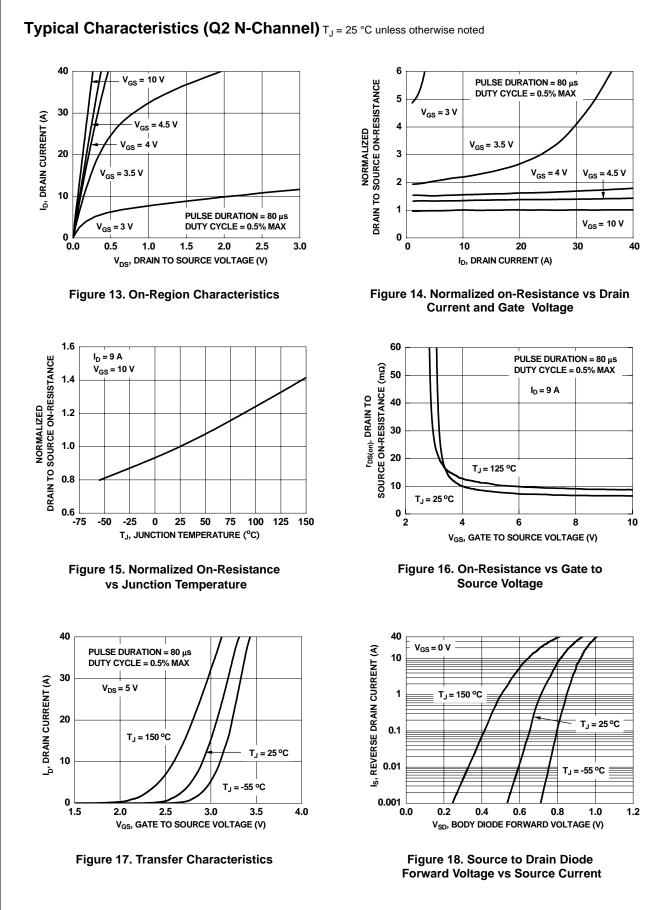
Typical Characteristics (Q1 N-Channel) T_J = 25 °C unless otherwise noted



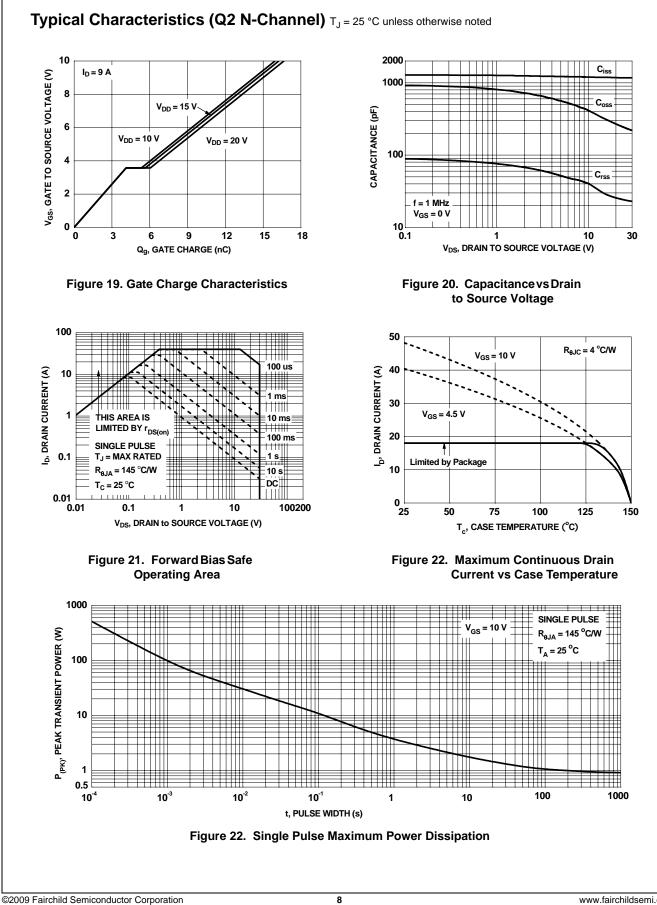




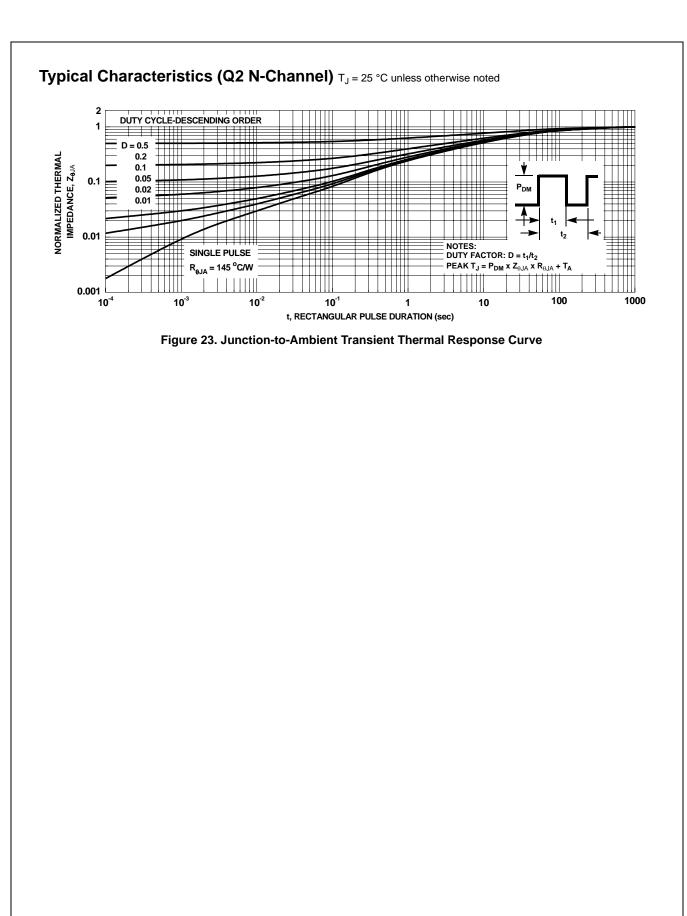
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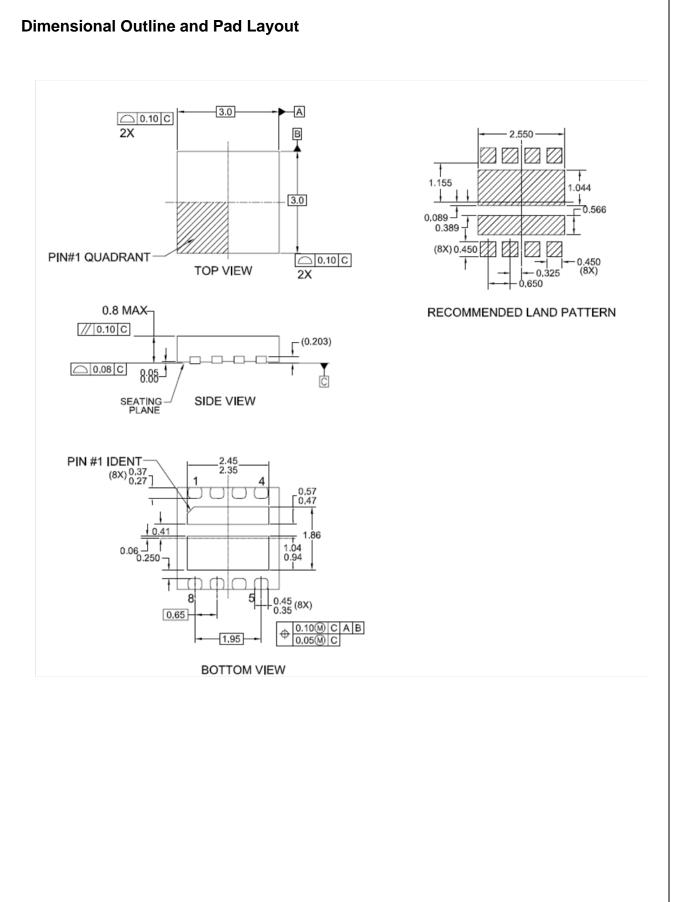














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